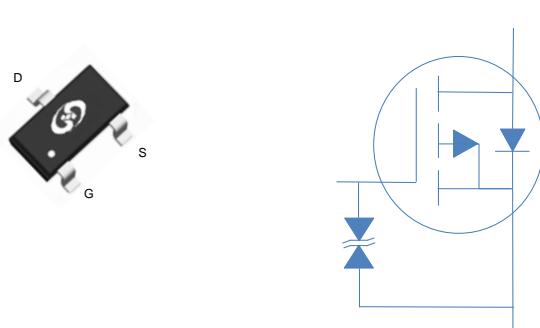


20V P-Ch Power MOSFET

V_{DS}	-20	V
$R_{DS(on),typ}$	$V_{GS}=4.5V$	37
$R_{DS(on),typ}$	$V_{GS}=2.5V$	55
$R_{DS(on),typ}$	$V_{GS}=1.8V$	65
I_D (Silicon Limited)	-4	A

Part Number	Package	Marking
HTJ440P02E	SOT-23	2E



Absolute Maximum Ratings at $T_J = 0$ °C

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_A	-4	A
		T_A	-3.5	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	± 8	V
Pulsed Drain Current	I_{DM}	-	-16	A
Power Dissipation	P_D	T_A	1.25	
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	R_{JA}	100	
Thermal Resistance Junction-Lead	R_{JL}	55	

Electrical Characteristics at $T_J = 0^\circ C$
Static Characteristics

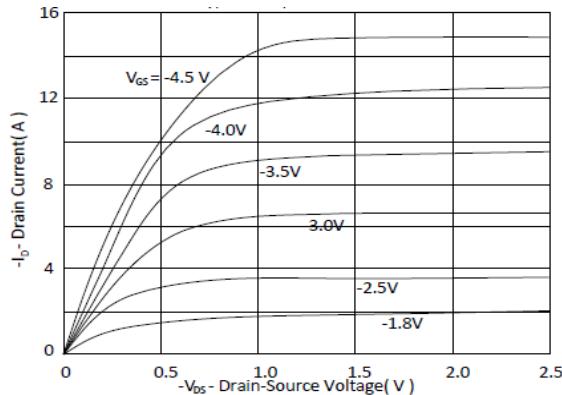
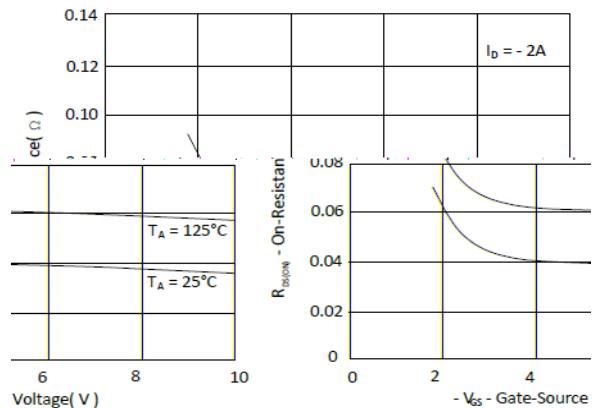
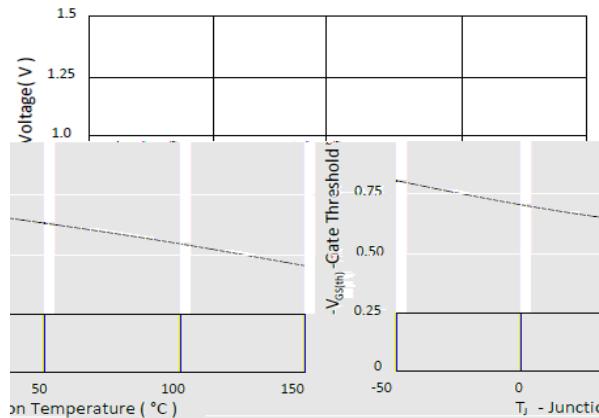
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250A$	-0.3	-0.65	-1.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-16V, T_j$	-	-	-1	A
		$V_{GS}=0V, V_{DS}=-16V, T_j$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V$	-	-	± 10	A
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-4A$	-	37	44	m
		$V_{GS}=-2.5V, I_D=-3A$		55	70	
		$V_{GS}=-1.8V, I_D=-1A$	-	65	90	
Transconductance	g	$V_{DS}=-5V, I_D=-4A$	-	14	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS} = 0$	-	1059	-	pF
Output Capacitance	C_{oss}		-	132	-	
0 0	C_{rss}		-	127	-	
Total Gate Charge	Q_g	$V_{DD}=-10V, I_D=-4A, V_{GS}=-4.5V$	-	12.9	-	nC
Gate to Source Charge	Q_{gs}		-	1.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.2	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-1A, V_{GS}=-4.5V, R_G=6\Omega$	-	15	-	ns
Rise time	t_r		-	30	-	
0 0 0	t		-	35	-	
Fall Time	t		-	35	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_F=-3A$	-		-1.2	V
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Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. Gate Threshold Voltage v.s. Junction Temperature


0 0 0 0 0 0

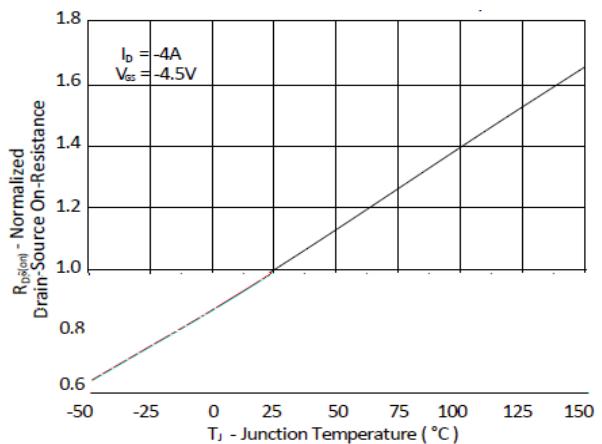
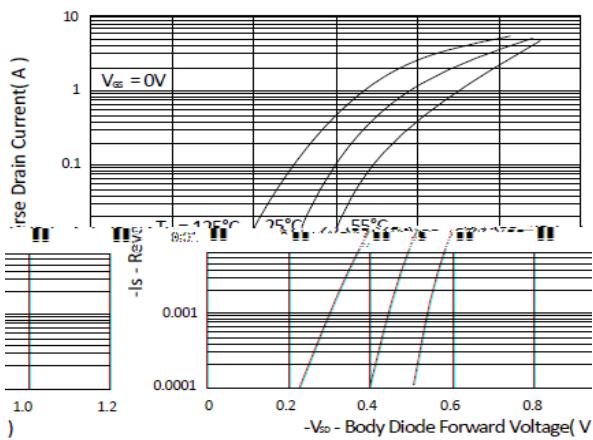

Figure 5.Typical Source-Drain Diode Forward Voltage


Figure 6.Typical Gate-Charge vs. Gate-to-Source Voltage

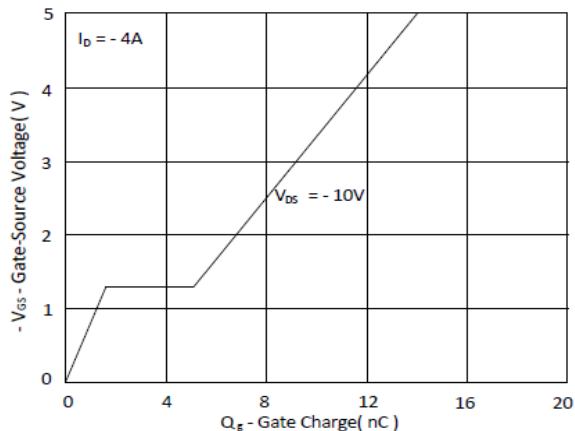
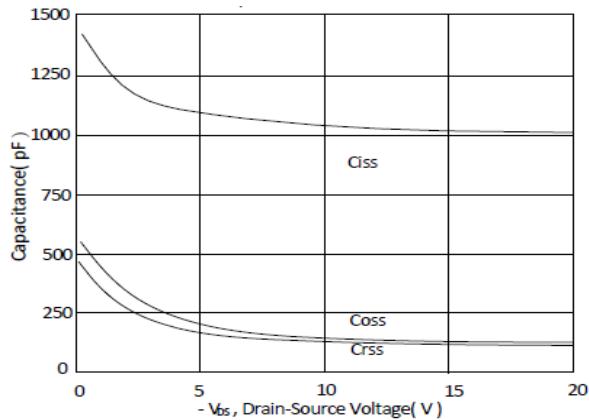
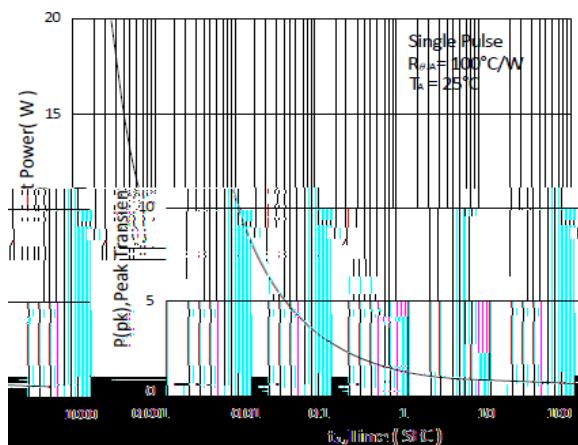
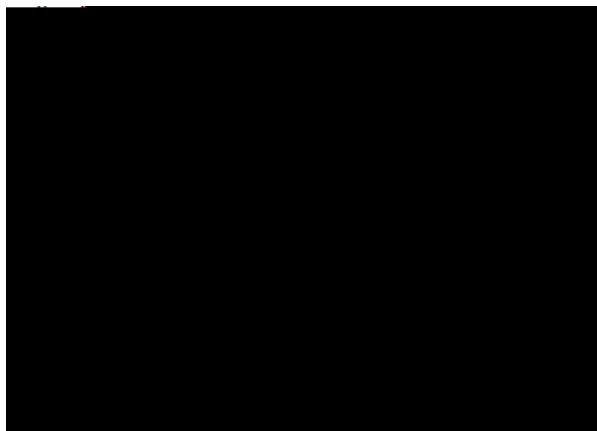


Figure 7. Typical Capacitance vs. Drain-to-Source Voltage

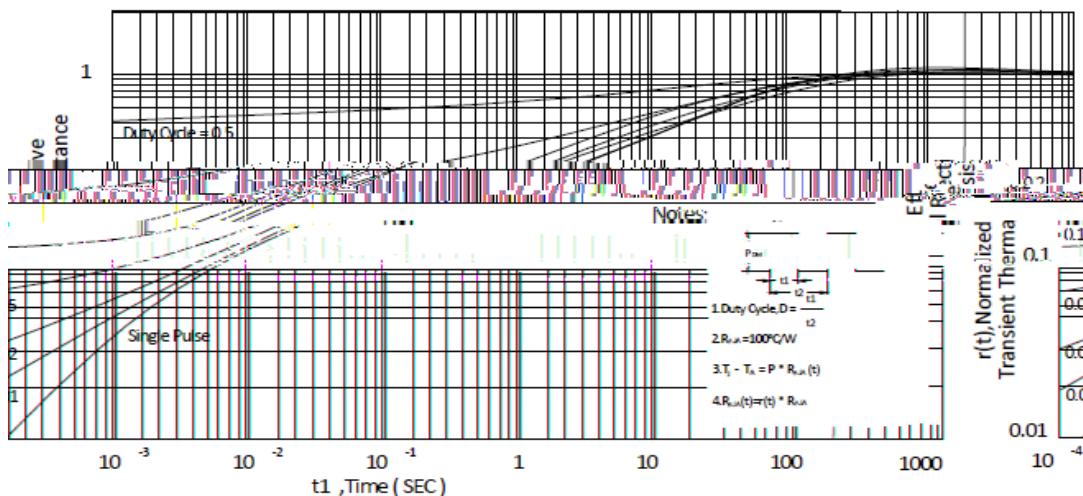


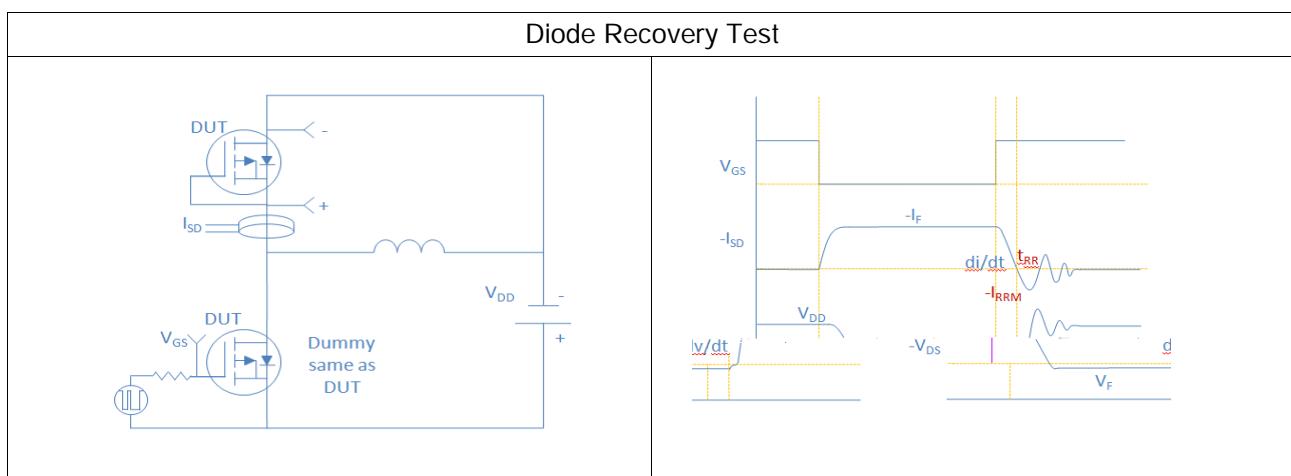
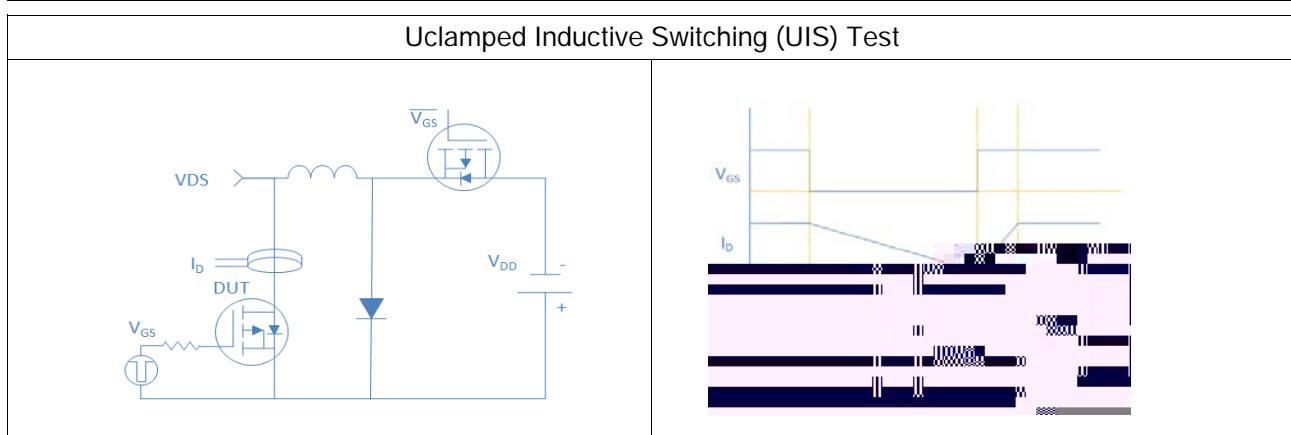
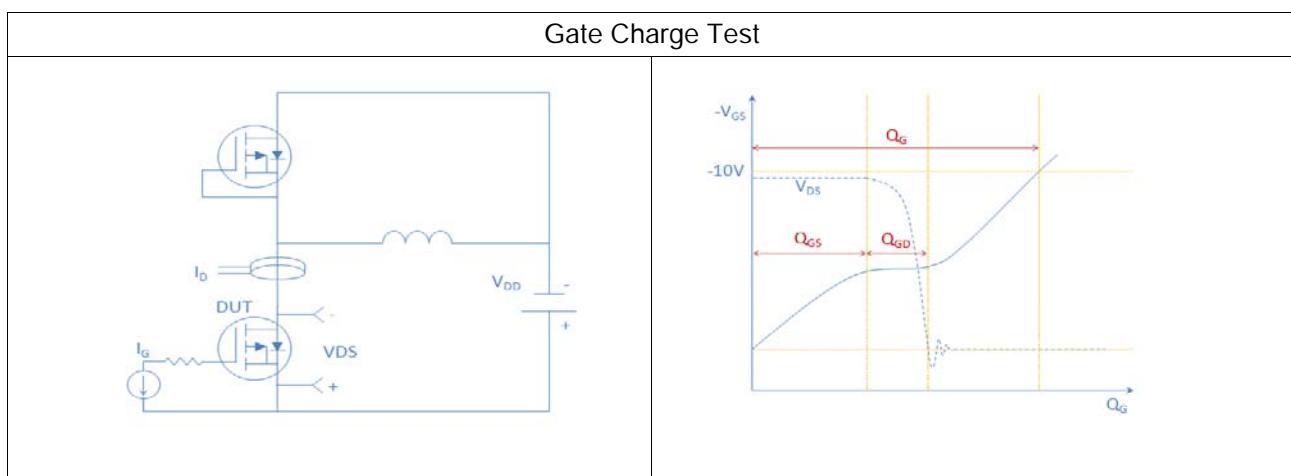
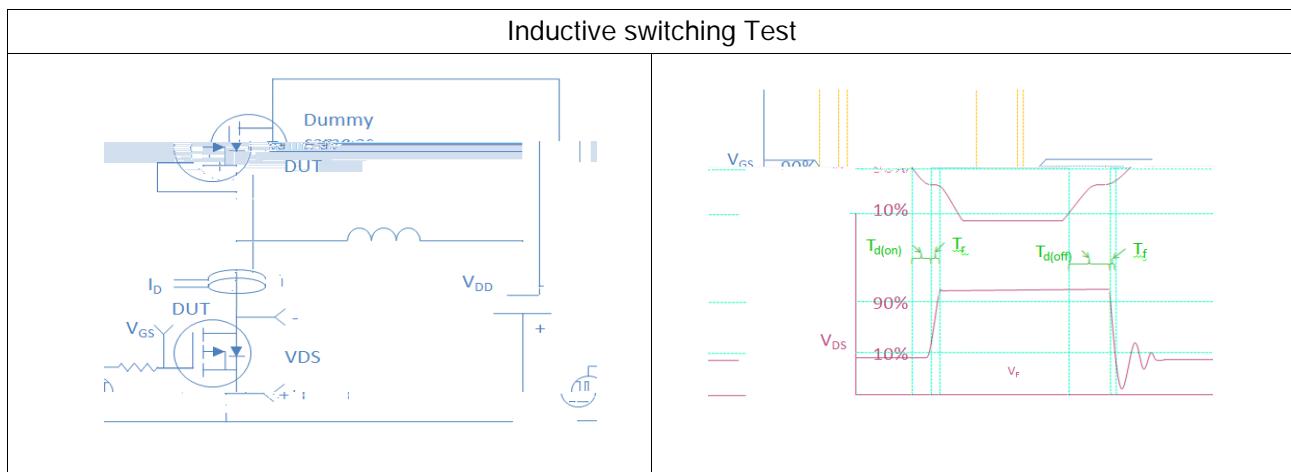
0 0 0 0

Figure 9. Single Pulse Maximum Power Dissipation



0 0 0 0 0





Packag Outl